We claim:

1. A multithreaded very large instruction word (VLIW) processor, comprising:

a plurality of functional units for executing instructions from a multithreaded instruction stream, said instructions being grouped into instruction packets by a compiler; and

an allocator that selects instructions from said instruction stream and forwards said instructions to said plurality of functional units, said allocator assigning instructions from at least one of said instruction packets to a plurality of said functional units.

2. The multithreaded very large instruction word (VLIW) processor of claim 1, wherein said allocator assigns as many instructions from a given instruction packet as permitted by an availability of said functional units.

3. The multithreaded very large instruction word (VLIW) processor of claim 1, further comprising a register for storing for execution in a later cycle an indication of those instructions from a given instruction packet that cannot be allocated to a functional unit in a given cycle.

4. The multithreaded very large instruction word (VLIW) processor of claim 3, wherein instruction packets in which all instructions have been issued to functional units are updated from the instruction stream of said thread.

5. The multithreaded very large instruction word (VLIW) processor of claim 3, wherein instruction packets with instructions indicated in said register are retained.

6. The multithreaded very large instruction word (VLIW) processor of claim 1, wherein said allocator can split an instruction packet provided the semantics of the instruction packet assembled by the compiler are not violated.

7. The multithreaded very large instruction word (VLIW) processor of claim 1, wherein said allocator can split an instruction packet provided a source register for one of the instructions

in a first part of said packet is not modified by one of the instructions in a second part of said packet.

8. A method for processing instructions in a multithreaded very large instruction word (VLIW) processor, comprising the steps of:

executing said instructions using a plurality of functional units, wherein said instructions are grouped into instruction packets by a compiler;

assigning instructions from said instruction stream to said plurality of functional units, wherein instructions from at least one of said instruction packets are assigned to a plurality of said functional units; and

forwarding said selected instructions to said corresponding functional units.

9. The method of claim 8, wherein said assigning step assigns as many instructions from a given instruction packet as permitted by an availability of said functional units.

10. The method of claim 8, further comprising the step of storing for execution in a later cycle an indication of those instructions from a given instruction packet that cannot be allocated to a functional unit in a given cycle.

11. The method of claim 10, wherein instruction packets in which all instructions have been issued to functional units are updated from the instruction stream of said thread.

12. The method of claim 10, wherein instruction packets with instructions indicated in said register are retained.

13. The method of claim 8, wherein said assigning step can split an instruction packet provided the semantics of the instruction packet assembled by the compiler are not violated.

14.   The method of claim 8, wherein said assigning step can split an instruction packet provided a source register for one of the instructions in a first part of said packet is not modified by one of the instructions in a second part of said packet.

5   15.   An article of manufacture for processing instructions from an instruction stream having a plurality of threads in a multithreaded very large instruction word (VLIW) processor, comprising:

a computer readable medium having computer readable program code means embodied thereon, said computer readable program code means comprising program code means
10   for causing a computer to:

execute said instructions using a plurality of functional units, wherein said instructions are grouped into instruction packets by a compiler;

assign instructions from said instruction stream to said plurality of functional units, wherein instructions from at least one of said instruction packets are assigned to a plurality
15   of said functional units; and

forward said selected instructions to said corresponding functional units.

16.   A multithreaded very large instruction word (VLIW) processor, comprising:

a plurality of functional units for executing instructions from a multithreaded
20   instruction stream, said instructions being grouped into instruction packets by a compiler; and

an allocator that selects instructions from said instruction stream and forwards said instructions to said plurality of functional units, said allocator assigning instructions from at least one of said instruction packets to a plurality of said functional units provided the semantics of said instruction packet assembled by said compiler are not violated.

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